I_{DDS}/V_P

CHAPTER

Field-Effect Transistors 5

5.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 and 4. Although there are important differences between the two types of devices, there are also many similarities that will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that the BJT transistor is a *current-controlled* device as depicted in Fig. 5.1a, while the JFET transistor is a *voltage-controlled* device as shown in Fig. 5.1b. In other words, the current I_C in Fig. 5.1a is a direct function of the level of I_B. For the FET the current I will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 5.1b. In each case the current of the output circuit is being controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

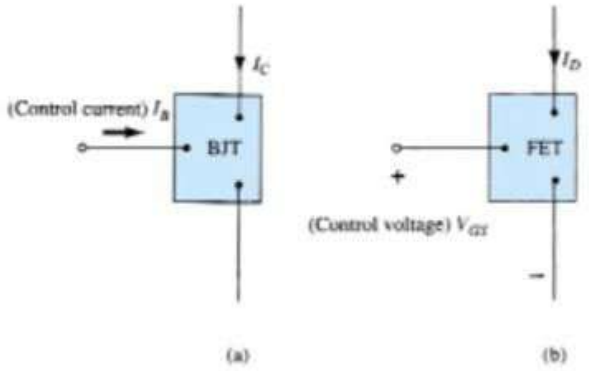

Figure 5.1 (a) Current-controlled and (b) voltage-controlled amplifiers.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi-* revealing that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term field-effect in the chosen name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to the magnet without the need for actual contact. The magnetic field of the permanent magnet has enveloped the filings and attracted them to the magnet through an effort on the part of the magnetic flux lines to be as short as possible. For the FET an *electric field* is established by the charges present that will control the conduction path of the output

I_{DSS}/V_P

circuit without the need for direct contact between the controlling and controlled quantities.

There is a natural tendency when introducing a second device with a range of applications similar to one already introduced to compare some of the general characteristics of one versus the other. One of the most important characteristics of the FET is its *high input impedance.* At a level of 1 to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than FETs for the same change in applied voltage. For this reason, typical ac voltage gains for BJT amplifiers are a great deal more than for FETs. In general, FETs are more temperature stable than BJTs, and FETs are usually smaller in construction than BJTs, making them particularly useful in *integrated-circuit (IC)* chips. The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Two types of FETs will be introduced in this chapter: the *junction field-effect transistor* (JFET) and the *metal-oxide-semiconductor field-effect transistor (MOSFET).* The MOSFET category is further broken down into depletion and enhancement types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section).

Once the FET construction and characteristics have been introduced, the biasing arrangements will be covered in Chapter 6. The analysis performed in Chapter 4 using BJT transistors will prove helpful in the derivation of the important equations and understanding the results obtained for FET circuits.

Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955. (Courtesy of AT&T Archives.)

Dr. Ross Born: Southport, England
PhD Gonville and Caius College, Cambridge
University President emeritus of AT&T Bell Labs Fellow—IEEE, Member of the National Science Board
Chairman—National Advisory Committee on Semiconductors

Dr. Dacey Born: Chicago, Illinois
PhD California Institute of Technology
Director of Solid-State Electronics Research at Bell Labs
Vice President, Research at Sandia Corporation
Member IRE, Tau Beta Pi, Eta Kappa Nu

5.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a section devoted to the impact of using a *pnp* transistor. For the JFET transistor the *n*-channel device will appear as the prominent device, with paragraphs and sections devoted to the impact of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 5.2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D),* while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).* The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p-n* junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig. 5.2 that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is that region void of free carriers and therefore unable to support conduction through the region.

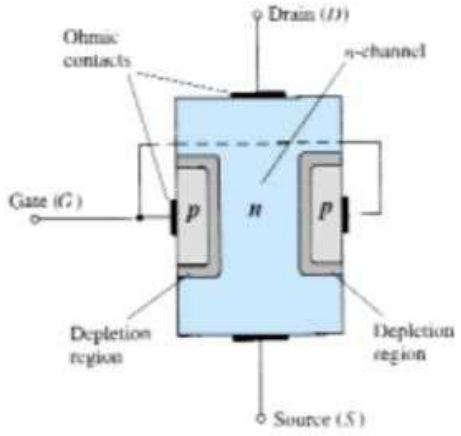

Figure 5.2 Junction field-effect transistor (JFET).

Analogies are seldom perfect and at times can be misleading, but the water analogy of Fig. 5.3 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source that will establish a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 5.2 because the terminology is defined for electron flow.

Figure 5.3 Water analogy for the JFET control mechanism.

$V_{GS} = 0$ V, V_{DS} Some Positive Value

In Fig. 5.4, a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 5.2. The instant the voltage V_{DD} ($= V_{DS}$) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 5.4. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions appearing in Fig. 5.4, the flow of charge is relatively uninhibited and limited solely by the resistance of the *n*-channel between drain and source.

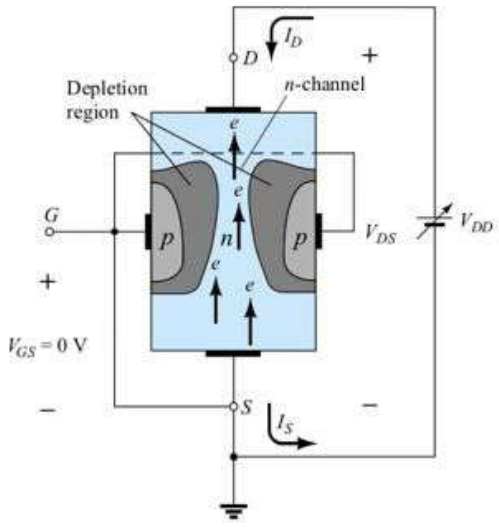

Figure 5.4 JFET in the $V_{GS} = 0$ V and $V_{DS} > 0$ V.

I_{DDS}/V_P

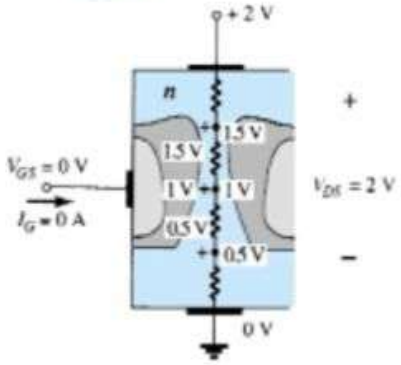

Figure 5.5 Varying reverse-bias potentials across the *p-n* junction of an *n*-channel JFET.

It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 5.5. Assuming a uniform resistance in the *n*-channel, the resistance of the channel can be broken down to the divisions appearing in Fig. 5.5. The current I_D will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the *p*-type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider the depletion region—hence the distribution of the depletion region as shown in Fig. 5.5. The fact that the *p-n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes as shown in the same figure. The fact that $I_G = 0$ A is an important characteristic of the JFET.

As the voltage V_{DS} is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 5.6. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 5.6, the depletion regions of Fig. 5.4 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 5.6 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig. 5.7, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P as shown in Fig. 5.6. In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 5.6, however, this is hardly the case—I_D maintains a saturation level defined as I_{DSS} in Fig. 5.6. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 5.6 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p-n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

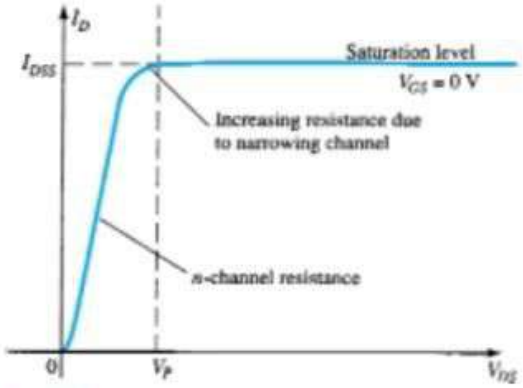

Figure 5.6 I_D versus V_{DS} for $V_{GS} = 0$ V.

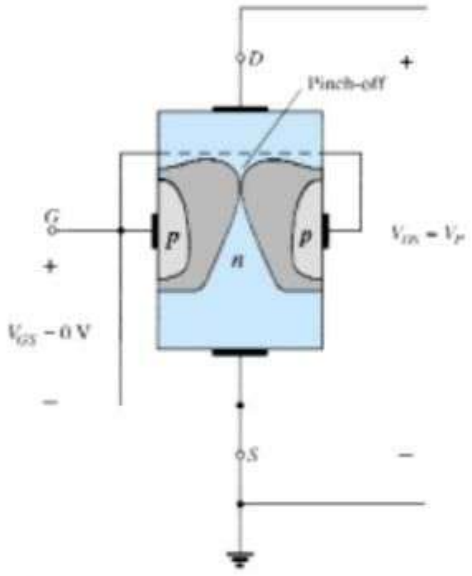

Figure 5.7 Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source. As shown in Fig. 5.8, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $> V_P$) is determined by the applied load.

The choice of notation I_{DSS} is derived from the fact that it is the *D*rain-to-*S*ource current with a *S*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.

Note in Fig. 5.6 that $V_{GS} = 0$ V for the entire length of the curve. The next few paragraphs will describe how the characteristics of Fig. 5.6 are affected by changes in the level of V_{GS}.

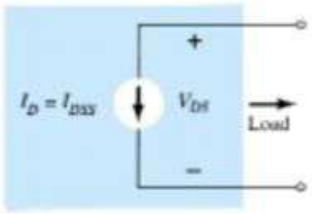

Figure 5.8 Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

$V_{GS} < 0$ V

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

In Fig. 5.9 a negative voltage of -1 V has been applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} as shown in Fig. 5.10 for $V_{GS} = -1$ V. The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also on Fig. 5.10 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

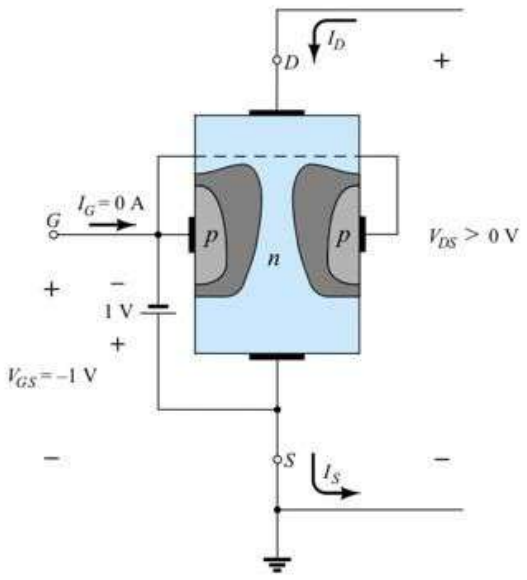

Figure 5.9 Application of a negative voltage to the gate of a JFET.

I_{DSS}/V_P

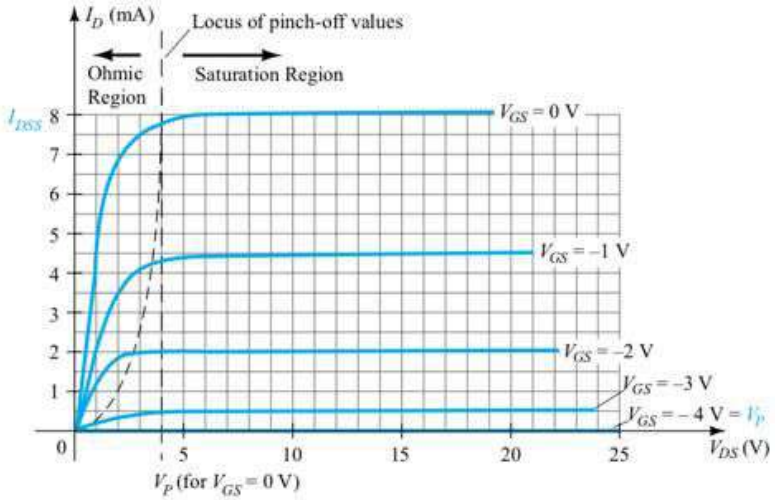

Figure 5.10 *n*-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

On most specification sheets the pinch-off voltage is specified as $V_{GS(off)}$ rather than V_P. A specification sheet will be reviewed later in the chapter when the primary elements of concern have been introduced. The region to the right of the pinch-off locus of Fig. 5.10 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 5.10 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 5.10 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ is a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level. The following equation will provide a good first approximation to the resistance level in terms of the applied voltage V_{GS}.

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \tag{5.1}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d the resistance at a particular level of V_{GS}.

For an *n*-channel JFET with r_o equal to 10 kΩ ($V_{GS} = 0$ V, $V_P = -6$ V), Eq. (5.1) will result in 40 kΩ at $V_{GS} = -3$ V.

p-Channel Devices

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 5.2, but with a reversal of the *p*- and *n*-type materials as shown in Fig. 5.11.

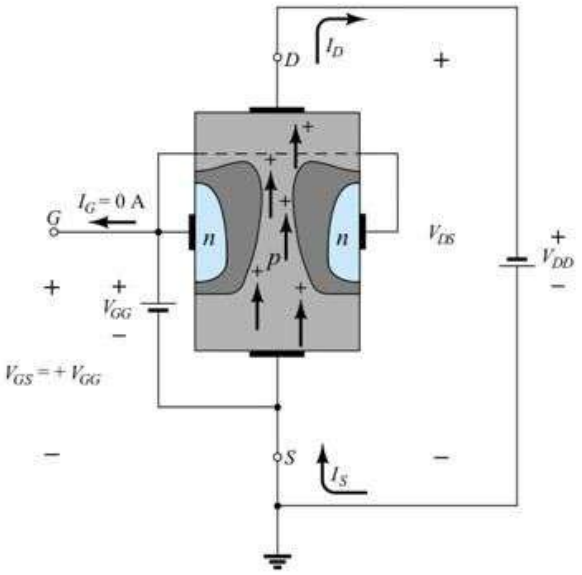

Figure 5.11 *p*-Channel JFET.

The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 5.12, which has an I_{DSS} of 6 mA and a pinch-off voltage of $V_{GS} = +6$ V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.

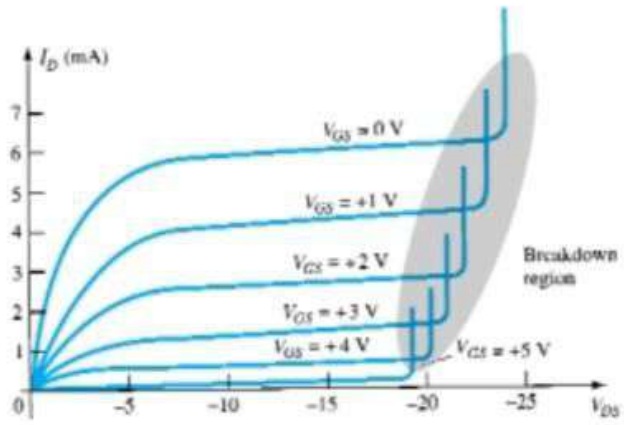

Figure 5.12 *p*-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 5.10 for the *n*-channel device, they do occur for the *n*-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS_{max}}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

I_{DDS}/V_P

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 5.13. Note that the arrow is pointing in for the *n*-channel device of Fig. 5.13a to represent the direction in which I_G would flow if the *p*-*n* junction were forward-biased. For the *p*-channel device (Fig. 5.13b) the only difference in the symbol is the direction of the arrow.

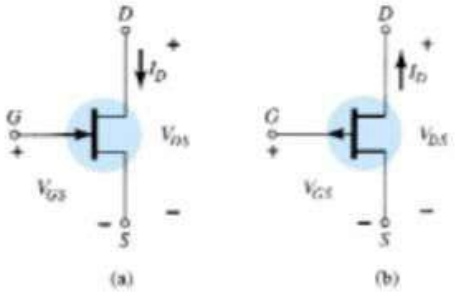

Figure 5.13 JFET symbols: (a) *n*-channel; (b) *p*-channel.

Summary

A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for *n*-channel JFETs include the following:

The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$ as shown in Fig. 5.14a.

For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A) as appearing in Fig. 5.14b.

For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as reviewed by Fig. 5.14c.

For p-channel JFETs a similar list can be developed.

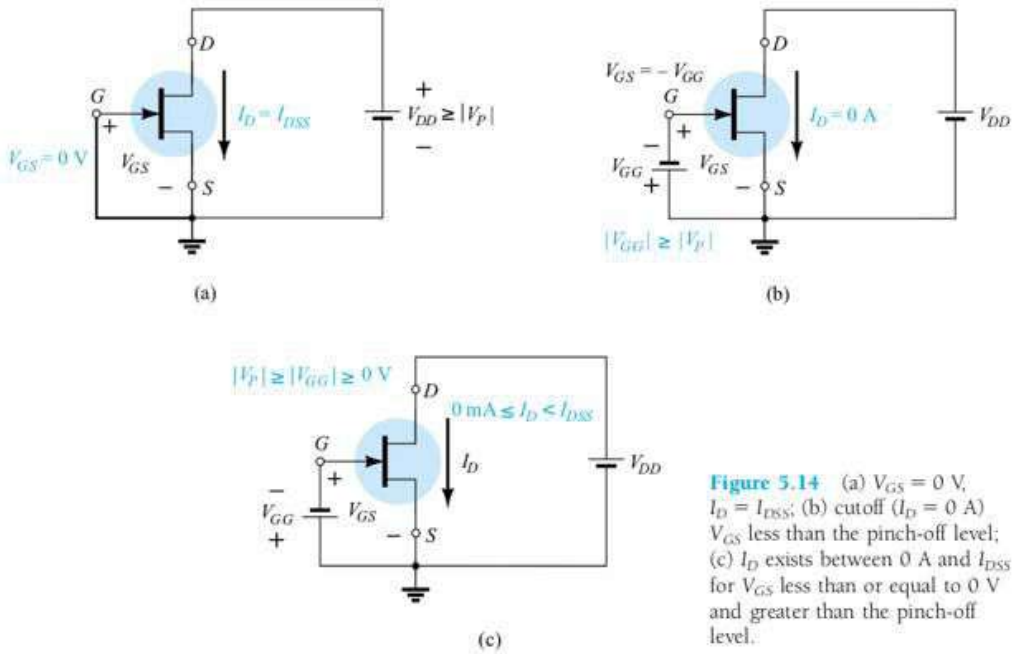

Figure 5.14 (a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D exists between 0 A and I_{DSS} for V_{GS} less than or equal to 0 V and greater than the pinch-off level.